In re Patent Application of:
MARIAUD ET AL.
Serial No. **09/989,317**
Filing Date: **NOVEMBER 20, 2001**

REMARKS

The Examiner is thanked for the thorough examination of the present application. Independent Claims 5, 11, 17, 20 and 22 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found on pages 3-4 of the originally filed specification, for example. No new matter is being added.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a computer system. As recited in amended independent Claim 5, for example, the computer system includes a master apparatus and a slave apparatus for communicating therewith via a universal serial bus (USB) protocol. The slave apparatus includes a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon, and a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from the sending/receiving circuit and supplying state signals of the sending/receiving circuit based thereon. The slave apparatus further includes a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by the sending/receiving circuit. Furthermore, an interruption state latch and a control circuit

cooperating therewith supply an interruption signal to the microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor is unavailable.

As such, the slave apparatus in accordance with the present invention may advantageously allow, at the end of a message, an acceptance of the start of a following message while the microprocessor is unavailable, without the need for re-sending the start of the message. Independent Claim 11 is directed to a similar computer system, independent Claim 17 is directed to a similar slave apparatus, and independent Claims 20 and 22 are directed to related methods. Each of these claims has been amended to recite that the interrupt signal is supplied to (or generated for) the microprocessor when the microprocessor is unavailable, similar to Claim 5.

II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 11, 17, 20 and 22 over the prior art discussed in the background of the present application (the "admitted prior art") in view of Shiroshita et al. (U.S. Patent No. 5,892,894). The admitted prior art describes a typical master-slave computer system arrangement, such as the one illustrated in FIG. 1 of the present application. Beginning on page 2, line 29, it is noted that during different transfer stages between the master apparatus and the slave apparatus, there are provisions which allow the master apparatus to repeat its part of the message IN and OUT while the

microcontroller (i.e., microprocessor) of the slave apparatus is unavailable. If the phase that follows is a start phase and its microcontroller is unavailable, the slave apparatus returns no signal (no NAK, nor STALL, nor ACK signal), which is interpreted by the master apparatus as a transmission error. In such case the master apparatus resends the message.

Such an operation only appears if the time period during which the slave microcontroller is unavailable exceeds a time interval separating two consecutive messages. However, in high-speed data transfers, these time intervals between two messages are increasingly short. Yet, the microcontroller of the slave apparatus has to perform more and more tasks, while the time periods during which it is unavailable are longer and longer.

At the end of the transfer stages, an interruption of the microcontroller to process the part of the transmitted message may be requested. To this end, a flag CTR is set to the logic 1 state to indicate that an interruption is requested (see FIG. 3(d) of the present application). After a certain time (which depends on the application), the interruption requested by the USB bus is processed. At the end of the interruption, the program executed by the microcontroller returns the flag CTR to the logic 0 state, thus authorizing the transfer of the following part of the message. A software state machine then processes the information concerning the event of the USB message extracted by the interruption routine.

As a result of the above operations, no transfer over the USB bus is authorized when the flag is in the logic 1 state.

There is, therefore, a dependency between the time for processing an interruption and the time delay in accepting the following transfer, the time for processing the interruption being linked to the microcontroller's operating frequency. Further, the time delay between each transaction depends on the master apparatus in that if that time delay is shorter than the minimum time for processing an interruption by the microcontroller, the following transfer cannot be authorized. This can result in the failure of the transaction.

The Examiner correctly acknowledges that the admitted prior art fails to teach or fairly suggest generating an interrupt signal when the microprocessor is unavailable. However, the Examiner contends that Shiroshita et al. provides this noted deficiency. This patent is directed to a data re-transmission management scheme for a communication network. That is, Shiroshita et al. is directed to multipoint communications between a server and several clients and the problem of how to deal with a slower client without slowing faster ones when all of the clients have to be uniformly managed. In support of his contention, the Examiner points to the "busy notification" step **S101** illustrated in FIG. 8 and mentioned at col. 6, lines 34-38 of Shiroshita et al., which states that "[w]hen the server **100** receives the busy notification from the terminal **300-3** during the data transmission (step **S101**), the server **100** records the fact that the terminal **300-3** is in a busy state at the terminal state management unit **106** (step **S102**)."

The above-noted independent claims have been amended to recite that the interruption state latch and a control circuit cooperate for supplying an interruption signal to the

microprocessor once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor is unavailable. In stark contrast, the busy notification generated by a slow client in the Shiroshita et al. system is not an interrupt signal for the client's own microprocessor. The busy signal is not an interruption signal at all, but rather merely a signal that is supplied to the server to inform the server that the slow client is too busy to accept the given data transmission. Thus, not only is Shiroshita et al. directed to client-server communications rather than master-slave USB communications as recited in the above-noted independent claims, Shiroshita et al. simply fails to teach or fairly suggest supplying an interruption signal for the microprocessor of a slave apparatus once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor is unavailable. Accordingly, the rejection of the independent claims should be withdrawn.

Moreover, Shiroshita et al. teaches away from making the selective combination of references proposed by the Examiner. That is, Shiroshita et al. teaches re-transmitting an entire data transmission to a client that provides a busy signal, rather than attempting to store any portion of the data transmission at the busy client. See, e.g., col. 6, lines 45-61. Thus, one of ordinary skill in the art would have been taught away from trying to record the start of a new message at a slave apparatus while the microprocessor of the slave apparatus was unavailable (e.g., acting upon a previous interrupt signal). As such, there is simply no proper motivation or suggestion to combine the references as the Examiner proposes, and the rejection of the

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independent claims should be withdrawn for this reason as well.

Accordingly, since none of the prior art of record teaches or fairly suggests all of the features recited in independent Claims 5, 11, 17, 20 and 22, it is respectfully submitted that these claims are patentable. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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